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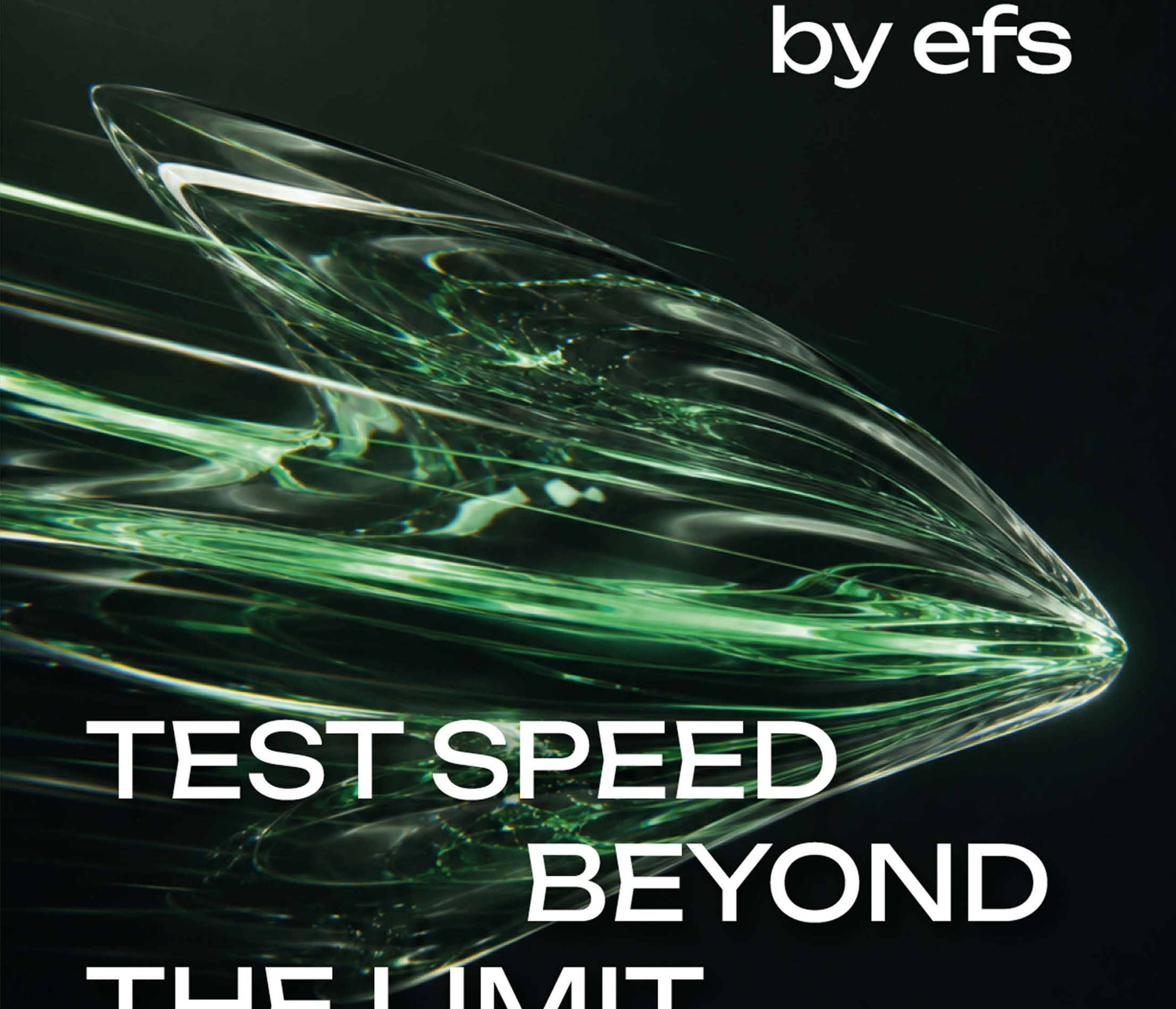
vPIL by efs



TEST SPEED BEYOND THE LIMIT

vPIL

INTRO

A virtualised PIL framework that decouples test software from the system under test and accelerates execution by factors well beyond 200x. Demonstrated 400x speed-up on ACF tests: from 8 days to under 30 minutes.

KEY FACTS

- → 200x+ speed-up of test execution; 400x measured on ACF tests.
- → Plug-and-play connectors for TPT, Google Test, C# and other frameworks.
- → Build artefacts (.o) executed without rebuild. No manual wrapper code.
- → Interchangeable execution targets: QEMU, TriCore, STM32, ARM, x86/x64.
- → Scales horizontally in CI/CD. Runs on developer machines and build servers.

THE CHALLENGE

PIL boards are the bottleneck of every embedded test campaign.

WHERE TEAMS LOSE TIME

- → One physical PIL board per test PC. No parallel execution.
- → Test cycles measured in days, not minutes. Developer feedback loops broken.
- → CI/CD pipelines blocked by hardware scarcity.

THE SOLUTION

→ vPIL by efs

vPIL decouples test software from the system under test and lifts execution onto an abstracted layer. The execution unit (microcontroller, emulator, SIL) becomes freely interchangeable. Test execution accelerates by factors beyond 200x. Available as standalone tooling or as a plugin for PikeTec TPT.

TOOLS

- → OSLC
- → C#
- → TPT
- → Google Test

MIDDLEWARE

- → labelled vPIL

TARGETS

- → µC
  (*QEMU, TriCore, STM32)*
- → µP/SIL
  (*Linux, Windows)*

KEY CAPABILITIES I

01. VIRTUALISED PIL VIA QEMU

Run target software on QEMU instead of physical PIL hardware. Nightly tests parallelise across the CI pool without hardware bottlenecks.

02. PLUG-AND-PLAY CONNECTORS

Direct connection to TPT, Google Test, C# and OSLC. Existing test suites run on vPIL without rewriting.

KEY CAPABILITIES II

03. ZERO-OVERHEAD BINARY INTEGRATION

Compiled binary objects (.o) are converted into executable SUTs without rebuild. Wrappers and de/serialisers are generated automatically.

04. INTERCHANGEABLE EXECUTION TARGETS

Seamless switch between microcontroller, emulator and SIL without changes to tests or SUT. Same test, different target, identical results.

SPECIFICATIONS & USE CASES

TECHNICAL SPECIFICATIONS

HARDWARE TARGETS
→ TriCore
→ STM32
→ ARM
→ QEMU emulation

SOFTWARE TARGETS
→ Linux and Windows on x86/x64

TOOL INTEGRATION
→ TPT
→ Google Test
→ C#
→ OSLC

SPEED-UP
→ 200x+ typical
→ 400x measured
(ACF tests: 8 days → 30 min)

DEPLOYMENT
→ Standalone tooling or plugin for PikeTec TPT

EXECUTION MODES
→ Local on developer machine
→ Distributed on build server

USE CASE
NIGHTLY TESTS ON THE BUILD SERVER

Replace the single physical PIL board with virtualised execution. Nightly regression runs in parallel across the CI pool.

USE CASE
DEVELOPER-SIDE EXECUTION

Developers run release tests on their own machine with the same compiler and target as the series build. Defects caught before commit.

USE CASE
CLOSED-LOOP SIMULATION

Embed the SUT in a custom closed-loop simulation environment. Timing measurements against real input data, without a hardware bench.

Development
Automated Driving Functions

Development
Chassis Control Systems

Real-world driving tests with
*Lean**DRA***

Diagnosis & data acquisition with
UDS-Whisperer

SUPERB
DATA KRAKEN

END-TO-END VERIFICATION WITH IDENTICAL TESTS AND CONSISTENT DATA FLOW

1 **SOFTWARE DEVELOPMENT**

Software design & implementation

Unit & component tests

2 **VIRTUAL DEVELOPMENT**

Requirements-based simulation environment

Standardised test process

3 **TEST AUTOMATION**

Testing with real hardware

vPIL

MIL / SIL / PIL / HIL

4 **SYSTEM INTEGRATION**

System integration & calibration

Integration & system tests

5 **TEST ENVIRONMENT**

Data analysis

Validated data

6 **TRACK-IN-THE-LOOP**

Track-in-the-loop / operational validation

Continuous validation

MODEL-BASED SYSTEMS ENGINEERING

AI METHODS AS ENABLERS

(test design, anomaly detection, data analytics, predictive analytics, scenario generation)

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